REMARKS/ARGUMENTS

The present application discloses a method, apparatus and program product for a self-healing, reconfigurable logic emulation system, wherein if a signal wire becomes faulty in an emulation cable during an emulation run, the runtime software can automatically reconfigure the emulator to reroute the data destined from the faulty signal wire across a spare wire. Such a feature enables a user to restart the emulation run without having to recompile the simulation model in order to account for the hardware fault.

Reconsideration of the application, as amended, is requested. Claims 3 and 13 have been amended. No new matter has been added. Claims 1-16 remain pending in this application.

In section 2 of the Office Action, the Examiner objects to claim 3 because it is dependent upon itself. Claim 3 has been amended to overcome this objection.

In section 4 of the Office Action, the Examiner rejects claims 13-16 under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. In response, Applicants have amended claim 13 to now refer to a **tangible** computer-readable medium in order to overcome this rejection.

In section 6 of the Office Action, the Examiner rejects claims 1-16 under 35 U.S.C. §103(a) as being unpatentable over Swoboda (U.S. Patent 6,928,403) in view of Knox et al (U.S. Patent 5,448,572). Applicants respectfully traverse this rejection.

The Swoboda reference describes automatic detection of connectivity between an emulator and a target device in a debugger system (Abstract). The Knox et al. reference describes an apparatus and method whereby a single spare line can be used to replace any of several signal lines in a signal path (Abstract).

Claim 1 of the present invention discloses "an emulation cable having a plurality of signal wires, the plurality of signal wires comprising a plurality of regular signal wires and **one or more spare signal wires.**" The Examiner states that the "one or more spare signal wires" are taught in Swoboda at column 10, lines 45-47, which states "It will be recognized that all pins of all chips need not necessarily be involved in the automatic connectivity check, but any or all of the pins may be."

Applicants respectfully submit that the passage cited by the Examiner neither discloses nor suggests the concept of "one or more spare signal wires," as claimed in the present invention. Firstly, the words "spare signal wires" do not literally appear in the passage cited by the Examiner. In fact, Applicants submit that the term "spare" does not literally appear anywhere within the cited patent. Furthermore, there are no other terms in the passage that Applicants feel are synonymous with "spare signal wires." Thus, Applicants submit that all wires used to connect pins in Swoboda are regular signal wires, not spare signal wires.

The passage cited by the Examiner refers explicitly to **pins**, not **wires**, which may or may not be connected to the pins. In fact, when the passage states that not all pins need to be involved in the connectivity check, this does not necessarily imply that there even are signal wires connected to those pins excluded from the connectivity check.

The passage cited by the Examiner actually teaches away from the concept of spare signal wires. If, in fact, all of the pins in the design under test are connected to signal wires, and all of the pins in the design are active, **there would be no unused wires that could even be potentially used as a spare signal wire**.

Also, even if there are unused regular signal wires, there is nothing in Swoboda which discloses or suggests that unused regular signal wires could be also be used as spare signal wires. As shown in Figure 2 of Swoboda, all connections are point-to-point chip-to-emulator (elements 22, 23, 24, and 25) or point-to-point chip-to-chip (element 26). There is no discussion of

alternative signal paths or multiplexers which will switch between bad signal paths to an alternative signal path. Thus, Applicants submit that there is no motivation in Swoboda that would cause one of skill in the art to combine the Swoboda reference with the Knox reference.

The Examiner concedes that Swoboda does not disclose expressly the runtime control program detecting faults on wires. The Examiner then further states that Knox discloses a method for "detecting a fault on a regular signal line, and reassigning the signal on the faulty line to a spare signal wire," as described in column 3, lines 4-10, shown below:

> Line 6 (215), the spare line, is normally not in use. If, in operation Line 3 (212) were to fail somewhere along the path shown, then by activating the selection line Sel 3 and 4 on multiplexers 204 and 205, the faulty line can be bypassed. Signals A and B still use their original signal lines, line 1 (210) and line 2 (211); signals C, D and E, are shifted to lines 4 (213), 5 (214) and 6 (215) respectively.

Applicants respectfully submit that there is nothing in the cited Knox passage which actually "detects" a fault on a regular signal line. It refers only to an operation that has already been determined to have failed, and the reassignment that occurs in light of the failure. In contrast to Knox, the present invention discusses a technique for detecting faults at runtime by sending patterns on the cables, then providing an automatic "patch" to the existing model, thus enabling the user to restart the current simulation job without having to recompile the simulation model (Specification, page 11, lines 12-18).

In light of the reasons stated above, Applicants respectfully submit that claim 1 is allowable over the cited Swoboda and Knox references, and should be passed to issuance. Applicants further submit that dependent claims 2-8 depend, either directly or indirectly, from claim 1, which is now submitted as allowable. Thus, for the same reasons, claims 2-8 are also now submitted as being in condition for allowance.

With regard to independent claims 9 and 13, the Examiner states that the claim element of "one or more predefined spare signal wires" is taught by Swoboda in column 10, lines 45-47, which states "It will be recognized that all pins of all chips need not necessarily be involved in the automatic connectivity check, but any or all of the pins may be."

Applicants respectfully submit that the passage cited by the Examiner neither discloses nor suggests the concept of "one or more predefined spare signal wires," as claimed in the present invention. Firstly, the words "spare signal wires" do not literally appear in the passage cited by the Examiner. In fact, Applicants submit that the term "spare" does not literally appear anywhere within the cited patent. Furthermore, there are no other terms in the passage that Applicants feel are synonymous with "spare signal wires." Thus, Applicants submit that all wires used to connect pins in Swoboda are regular signal wires, not spare signal wires.

The passage cited by the Examiner refers explicitly to **pins**, not **wires,** which may or may not be connected to the pins. In fact, when the passage states that not all pins need to be involved in the connectivity check, this does not necessarily imply that there even are signal wires connected to those pins excluded from the connectivity check.

The passage cited by the Examiner actually teaches away from the concept of spare signal wires. If, in fact, all of the pins in the design under test are connected to signal wires, and all of the pins in the design are active, **there would be no unused wires that could even be potentially used as a spare signal wire.**

Also, even if there are unused regular signal wires, there is nothing in Swoboda which discloses or suggests that unused regular signal wires could be also be used as spare signal wires. As shown in Figure 2 of Swoboda, all connections are point-to-point, chip-to-emulator (elements 22, 23, 24, and 25) or point-to-point, chip-to-chip (element 26). There is no discussion of alternative signal paths or multiplexers which will switch between bad signal paths to an

alternative signal path. Thus Applicants submit that there is no motivation in Swoboda that would cause one of skill in the art to combine the Swoboda reference with the Knox reference.

Finally, with regard to the claim element of "one or more predefined spare signal wires", the present invention predefines a "plurality of signal wires" having "a plurality of regular signal wires" and "one or more spare signal wires," specification, page 5, lines 16-17. Thus, the "plurality of regular signal wires" and "one or more spare signal wires" are simultaneously predefined as separate and distinct entities. By contrast, the Examiner is appearing to state with regard to Swoboda in column 10, lines 45-47, that any unused "regular signal wires" may be **re-defined** to "spare signal wires" if they are unused as regular signal wires. Thus, once again, the Swoboda reference teaches away from the present invention by **re-defining** regular signal wires as spare signal wires, while the present invention **pre-defines** separate and distinct, preexisting "regular" and "spare" signal wires, which are never re-defined.

In light of the reasons stated above, Applicants respectfully submit that claims 9 and 13 are allowable over the cited Swoboda and Knox references, and should be passed to issuance. Applicants further submit that dependent claims 10-12 and 14-16 depend, either directly or indirectly, from claims 9 and 13, which are now submitted as allowable. Thus, for the same reasons, claims 10-12 and 14-16 are also now submitted as being in condition for allowance.

In view of the foregoing comments and amendments, the Applicants respectfully submit that all of the pending claims (i.e., claims 1-16) are in condition for allowance and that the application should be passed to issue. The Examiner is urged to call the undersigned at the below-listed telephone number if, in the Examiner's opinion, such a phone conference would expedite or aid in the prosecution of this application.

I hereby certify that this correspondence is being electronically transmitted to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

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(Date of Deposit)

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Respectfully submitted,

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